

IC ASSEMBLY

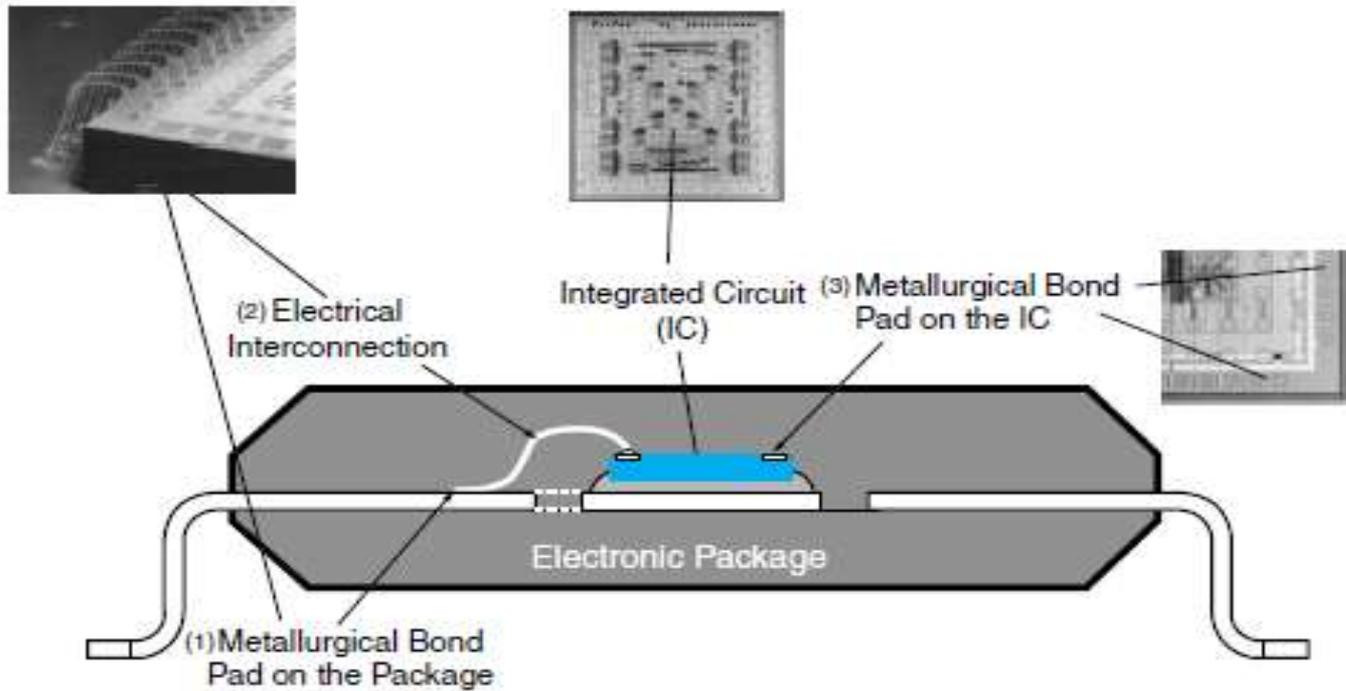
IC Assembly

- IC assembly – the first processing step after wafer fabrication and singulation that enables ICs to be packaged for systems use.
- Process of electrically connecting I/O bond pads on the IC to the corresponding bond pads on the package.
- Single chip package, multichip package, system level board.

Three interfaces:

- (1) Metallurgical bond pad interface on the IC
- (2) Metallurgical bond pad interface on the package
- (3) Electrical interconnection between these two interfaces

IC Assembly



Purpose of IC Assembly

Primary functions of IC assembly

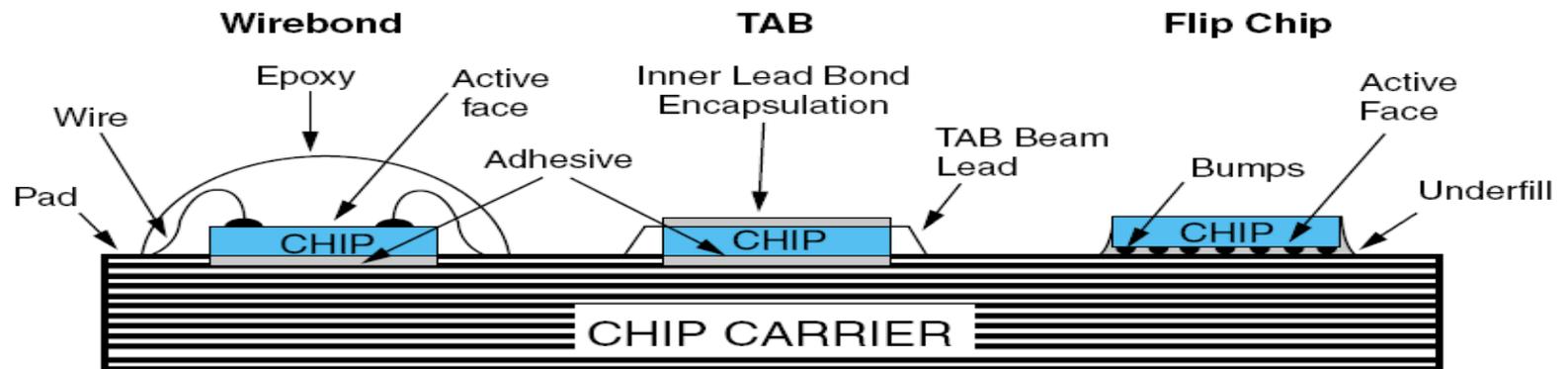
- (1) To provide signal and power distribution of the packaged IC to the system.
- (2) To provide mechanical support to fragile IC
- (3) To provide environmental protection of the IC

Requirements for IC Assembly

1. To provide acceptable electrical properties such as capacitance resistance, and inductance. (wire bonds have long lengths resulting in high impedance and longer signal delay times)
2. IC assembly technologies should provide a low cost solution for the electrical interface between the chip and package.
3. High Throughput manufacturing.
4. High Reliability. (Flip chip on ceramic technology has been a highly reliable interconnection technique)
5. Repairability where the interconnection between the IC and the package should provide replacement with a new high quality IC.

IC Assembly Technologies

- Chip-to-package accomplished using three primary interconnection technologies:
- Wirebonding
- Tape automated bonding (TAB)
- Flip chip



Two options:

- Ball bonding
- Wedge bonding

Two options:

- Face up chip
- Face down chip

Three options:

- Metallurgical bond
- Metallurgical and adhesive bond
- Adhesive bond

WIREBONDING

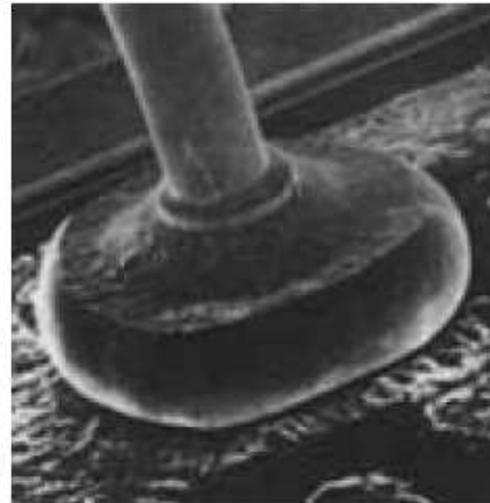
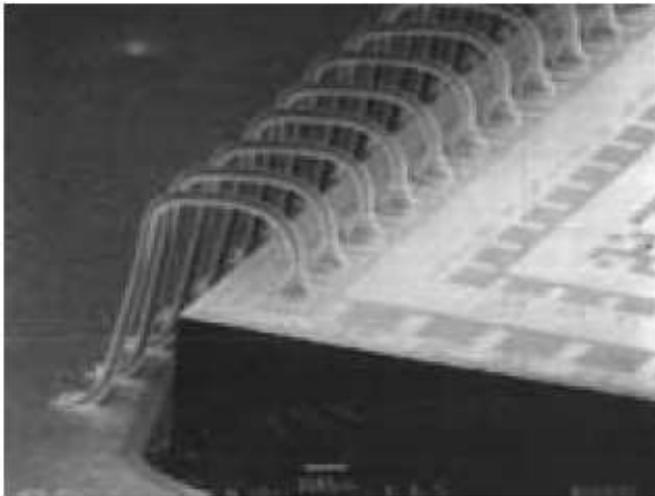
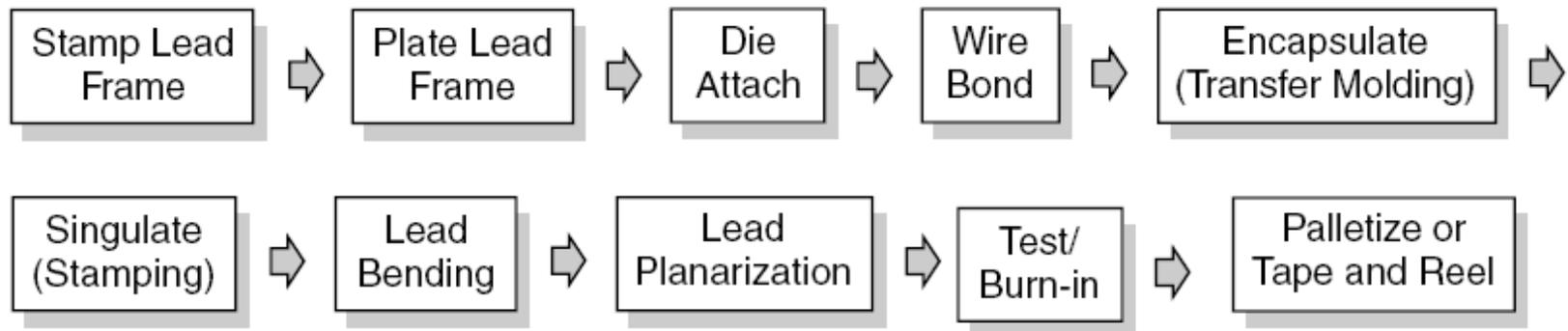
- Technology is originated with AT&T's beam lead bonding in 1950s
- Chip-to-package interconnection technique where fine metal is attached between each of the I/O pads on the chip, one at the time.
- Two major types of wirebonds: *gold ball bonding & aluminum wedge bonding*
- Focus on ball bonding, since it dominates this technology.
- Gold wire (25 μ m thickness) is bonded using ultrasonic bonding between the IC bond pad and the matching package pad.
- Well over 90% of all chip-to-package interconnections formed in 1999.

Advantages and disadvantages

- The advantages of wirebonding:
 - Highly flexible chip-to-package interconnection process
 - Low defect rates or high yield interconnection processing
 - Easily programmed
 - High reliability interconnection structure
 - Very large industry infrastructure supporting the technology
 - Rapid advances in equipment, tools, and material technology
- The disadvantages of wirebonding:
 - Slower interconnection rates due to point-to-point processing of each wirebond
 - Long chip-to-package interconnection lengths, degrading electrical performance
 - Larger footprint required for chip to package interconnection

Overall Processes

- Plastic packaging used worldwide



Overall Processes

- **Ball Bonding** – the most common technique (over 95%)
- **Wedge Bonding** – the finest pitch bonding capabilities, because the fact that the bonds can be formed by deforming the wire only 25-30% beyond the original diameter.

Fundamentals of Ultrasonic Bonding \

Theory states that ultrasonic energy allows the materials to plastically deform at much lower stress compared to pure thermal or mechanical energy.

- **Materials Used in Wirebonding** – gold for ball bonding and aluminum for wedge bonding. Typical wire diameter is 25 μ m.
- **Die Attach Materials** – solders, conductive adhesives, and glass adhesives.

Electrical Performance

- Of all of the chip-to-package interconnection types, the electrical performance is the lowest
- Long lengths of the wires interconnecting the chip and package lead frame.
- Lower electrical performance limited the use of wirebond interconnection in high speed applications.

Microprocessor	>	
High speed ASICs	>	flip chip
High speed memory	>	and
High speed RF	>	Tape Automated Bonding (TAB)
Analog	>	

Reliability/Failures

- Wirebond interconnection structures ➤ Very reliable
- Not used in high speed applications but used in space, automotive, medical, aerospace applications.
- Also used in low cost electronics: toys, smart cards, RF tags, AM-FM radios.
- Chip fracture, chip passivation cracking, chip metallization corrosion, wire sweep, cratering of wirebonding pad, bond fracture and lift-off, interfacial delamination, package cracking.
- Examples of plastic packages that are wirebonding are:
 - Thin small outline packages (TSOP)
 - Plastic quad flat packs (PQFPs)
 - Ball grid arrays (BGAs)
 - Chip scale packages (CSPs)

- **Wire bonding** is a method of making interconnections between an IC and other electronics as part of semiconductor device fabrication.
- The wire is generally made up of one of the following:

[Gold](#)

[Aluminum](#)

[Copper](#)

- Wire diameters start at 15 μ m and can be up to several hundred micrometers for high-powered applications.
- There are two main classes of wire bonding:

[Ball bonding](#)

[Wedge bonding](#)

- Ball bonding usually is restricted to gold and copper wire and usually requires heat. Wedge bonding can use either gold or aluminum wire, with only the gold wire requiring heat.
- In either type of wire bonding, the wire is attached at both ends using some combination of heat, pressure, and ultrasonic energy to make a weld.
- Wire bonding is generally considered the most cost-effective and flexible interconnect technology, and is used to assemble the vast majority of semiconductor packages.

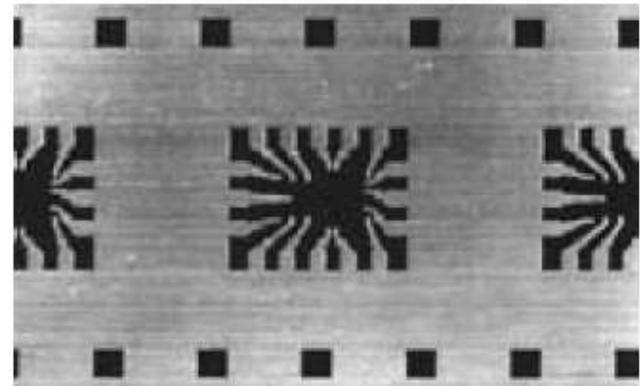
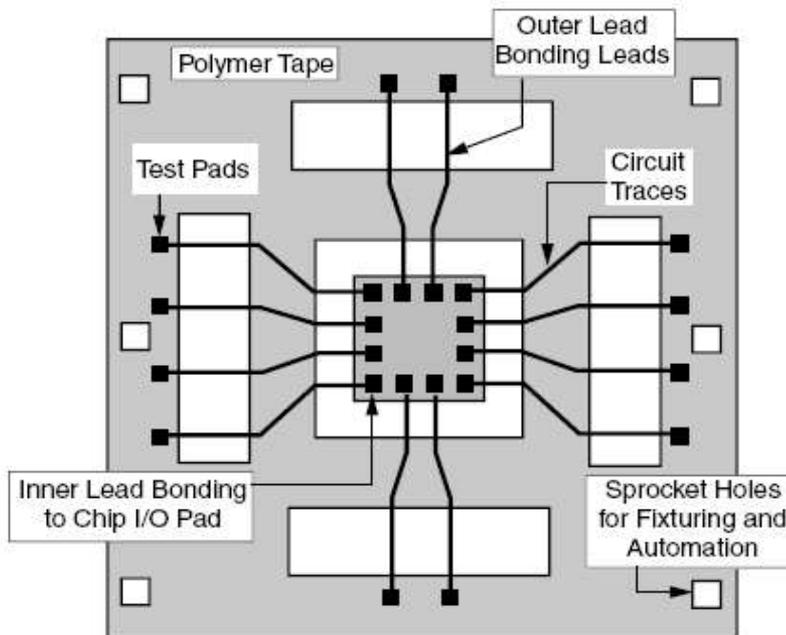
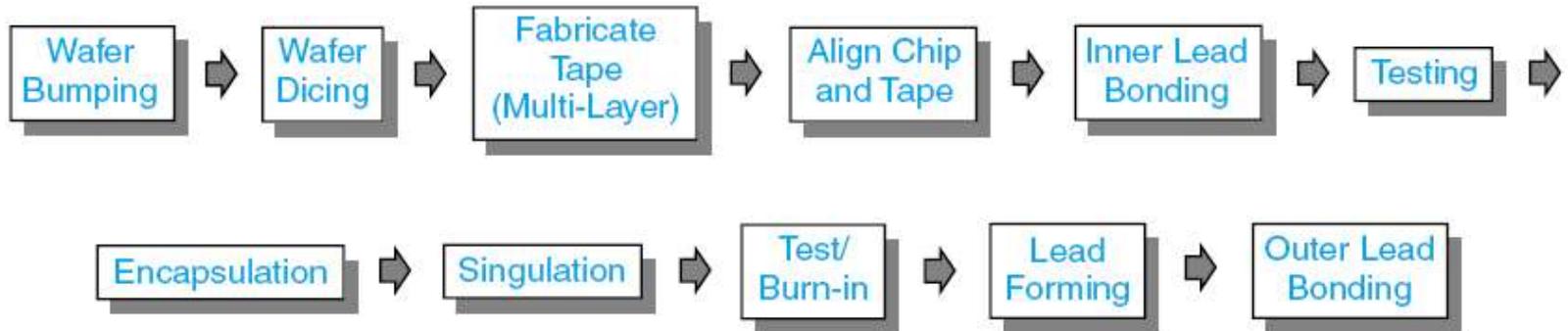
TAPE AUTOMATED BONDING

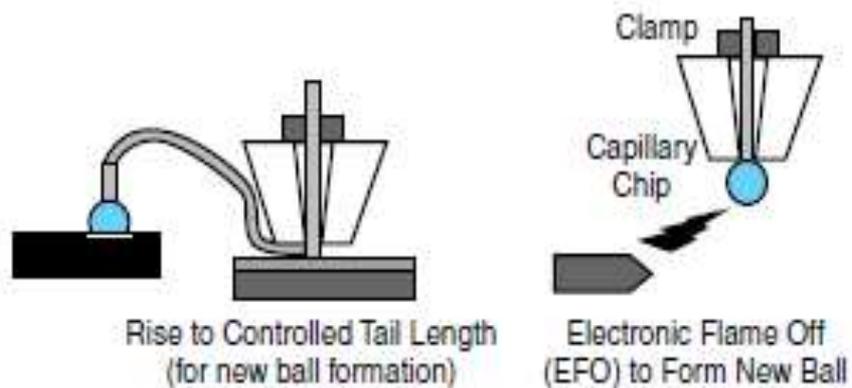
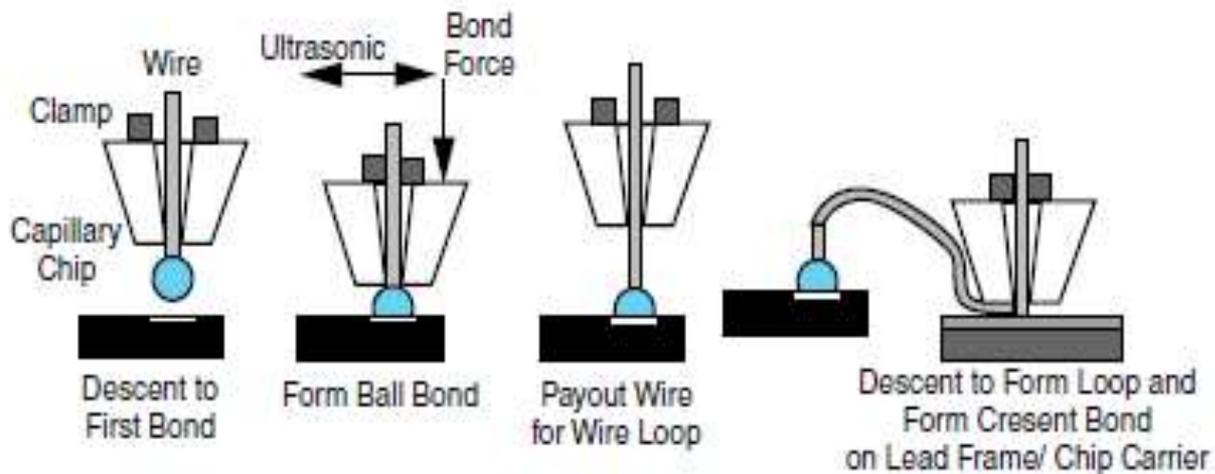
- IC assembly technique based on mounting and interconnecting ICs on metalized flexible polymer tapes.
- One end fully automated bonding of an etched copper beam lead to an IC, and other end of the lead to a PWB.
- 1966 – commercialized by General Electric Research Laboratory
First used in small-signal integration devices (1-40 transistors, 14 I/Os)
- 1970 – strong consideration and attention but little experienced expect in Japan
- 1980 – the most widespread adoption
- Up to now- used in high density I/O and high speed circuitry of VLSI
- Applied to variety of consumer, medical, security computer, peripheral, telecommunication, automotive and aerospace products.

Disadvantages

- Some of the advantages of TAB:
 - Ability to handle small bond pads and finer pitches on the IC
 - Elimination of large wire loops
 - Low profile interconnection structures for thin packages
 - Improved electrical performance
 - Ability to handle high I/O counts
 - Reduced weight
- Some of the disadvantages of TAB:
 - Package size tends to increase with larger I/O counts
 - Little production infrastructure
 - Difficulty in assembly rework
 - System testability
 - Large capital equipment investment required

Structure and Processes





Electrical performance

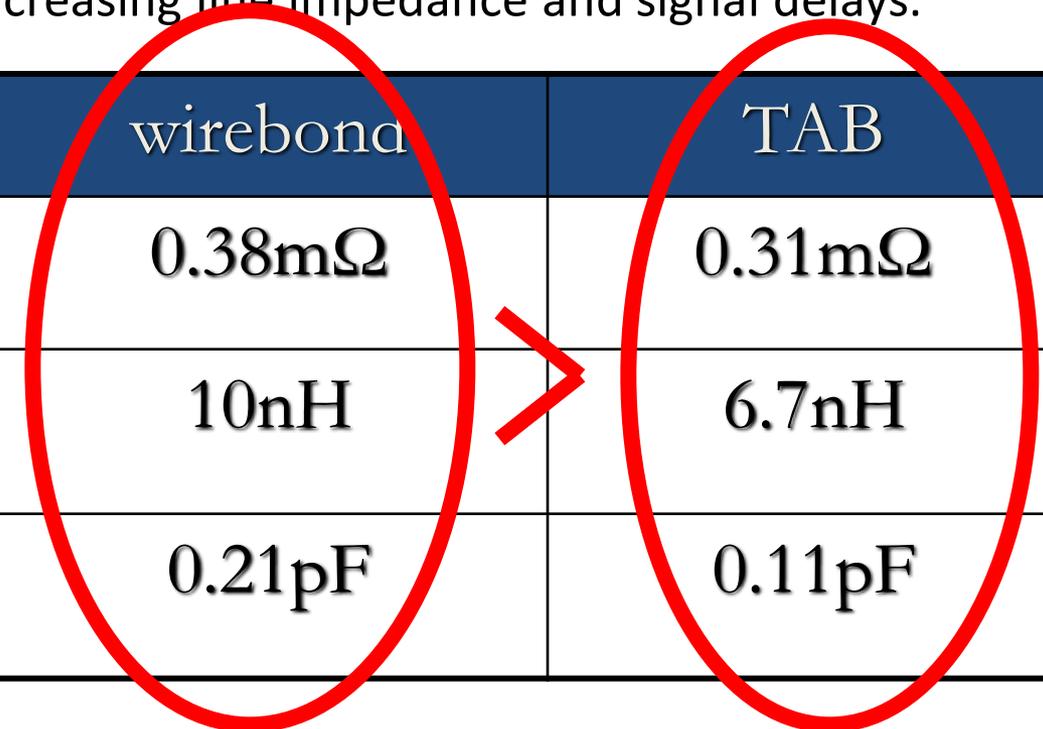
- TAB interconnections have improved electrical performance.
- Short circuit lead lengths between the chip and substrate reducing the impedance and signal delays.
- On the other side, wirebond have long wire loops between the chip and package lead frame, increasing line impedance and signal delays.

parameter	wirebond	TAB
Resistance	0.38m Ω	0.31m Ω
Inductance	10nH	6.7nH
Capacitance	0.21pF	0.11pF

Electrical performance

- TAB interconnections have improved electrical performance.
- Short circuit lead lengths between the chip and substrate reducing the impedance and signal delays.
- On the other side, wirebond have long wire loops between the chip and package lead frame, increasing line impedance and signal delays.

parameter	wirebond	TAB
Resistance	0.38mΩ	0.31mΩ
Inductance	10nH	6.7nH
Capacitance	0.21pF	0.11pF



Examples

- **Tape Ball Grid Array** – developed by IBM.
Area array first level interconnections and a standard ground plane
Lower lead inductance, lower power-supply inductance, lower signal delay
- **TapePak** – developed by National Semiconductor.
Fully testable, plastic model, quad-flat-pack
Leads on all four sides of the surface mountable package
- **Pentium TCP** – by Intel
For notebooks, laptops, palm top computers, related portable products.
- **ETA Supercomputer** – by ETA Systems
Implemented one of the first TAB applications in the 1970.
Packages were 248 pin quad flat packs.

Summary

- Tape Automated Bonding is an interconnect technology between the substrate and the IC, using a prefabricated carrier with copper leads adapted to the IC pads instead of single wires.
- Today TAB is well introduced in Japan and Taiwan and it features many benefits in applications like LCD drivers, high speed circuits, high pin count circuits or very low profile designs.
- Has better electrical performance than wirebonding technology.
- Microprocessors and ASICs benefit from TAB in the fields where high frequencies, high pin counts or high power dissipation are concerned.

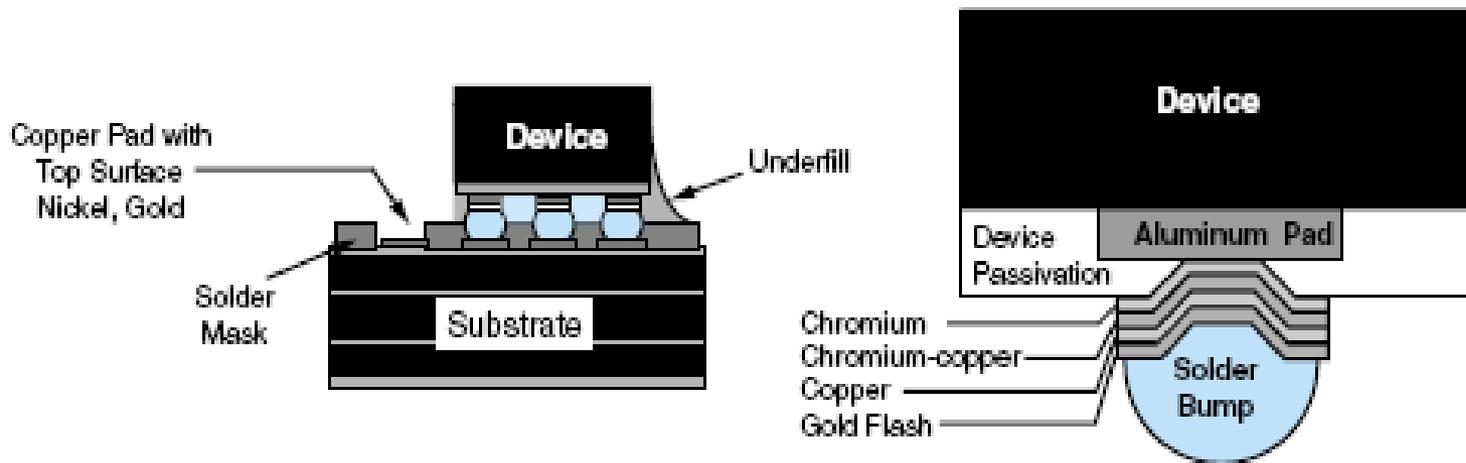
FLIP CHIP

- Developments to improve cost, reliability and productivity in the electronic packaging industry – flip chip technology.
- Introduced as the *Solid Logic Technology* by IBM in 1962.
- In 1970, converted into *Controlled Collapse Chip Connection (C4)*
- Flip chip = Advanced form of SMT, in which bare semiconductor chips are turned upside down and bonded directly to PCB.
- Initially applied to peripheral contacts, but quickly progressed to area arrays which allow for high I/O counts at larger pitches.



Concept

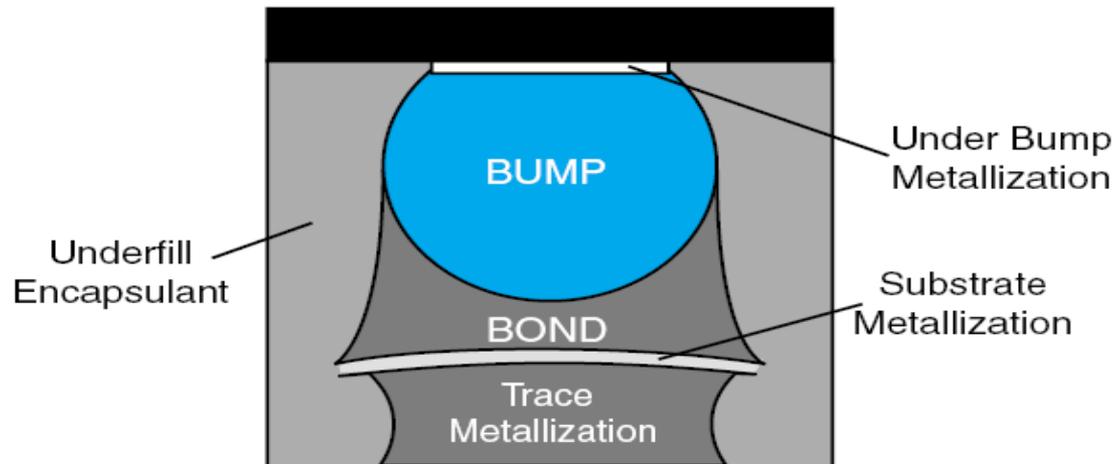
- Flip chip is the connection of an integrated circuit chip to a carrier or substrate with the active face of the chip facing toward the substrate.
- The basic structure of flip chip consists of an IC or chip, an interconnection system, and a substrate.



- The IC can be made of silicon, gallium-arsenide, indium-phosphide.
- Substrate material could be ceramic, epoxy-glass laminate, ceramic thick-film and many more

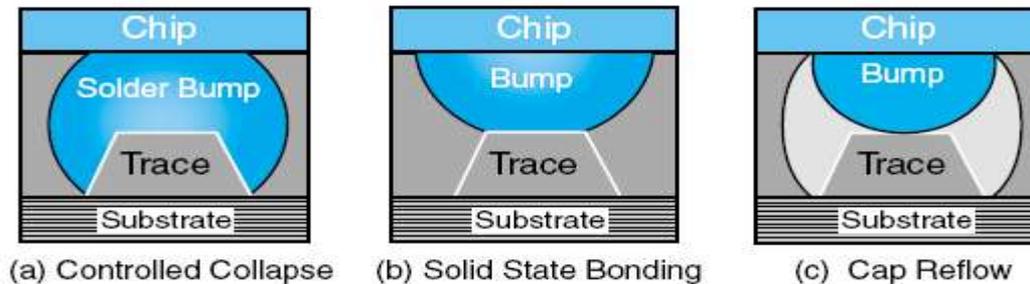
IC Bond Pad Interface

- The interconnection system is subdivided into four functional areas:
 - Under bump metallization (UBM)
 - Chip bumps
 - Encapsulation
 - Substrate metallization



Flip Chip Processing

- Solder Interconnection Processing
 - (a) Wetted controlled Collapse solder interconnection (High Temp.)
 - (b) Solid state bond (Similar to wirebonds)
 - (c) Cap reflow configuration (Two metals)



- Isotropic and compressed anisotropic Adhesives

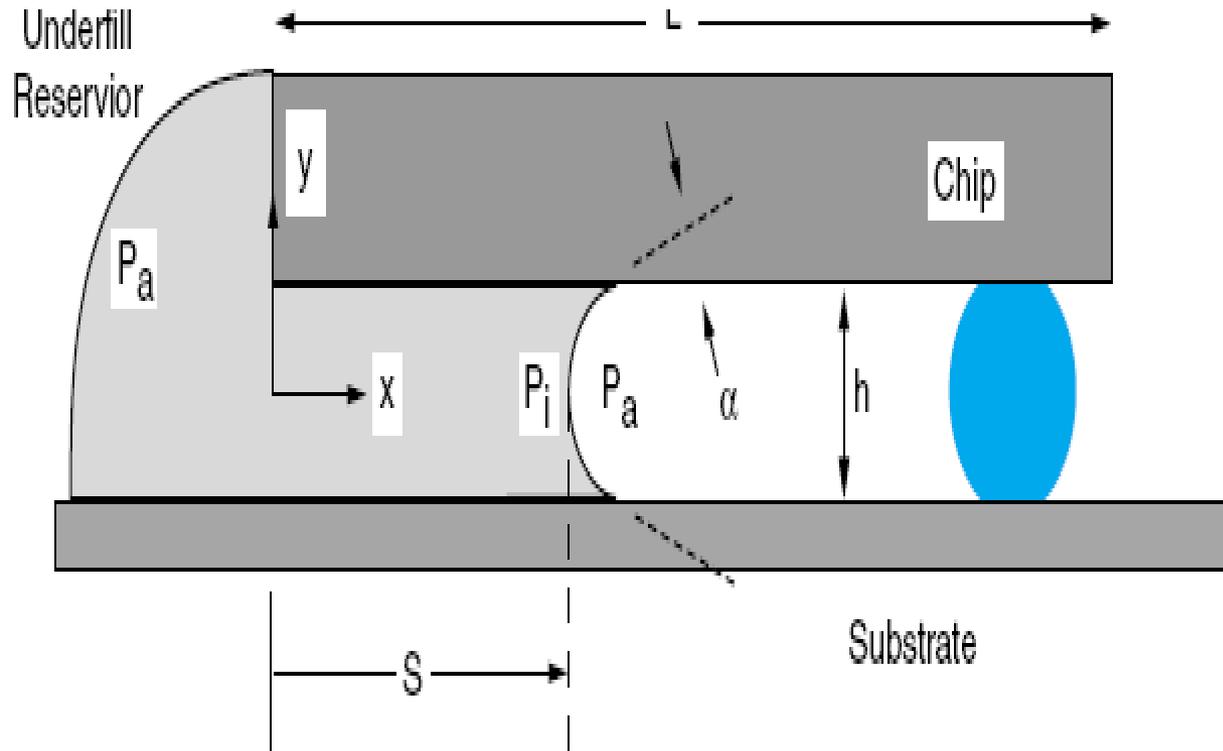
Flip Chip on Organic Substrate

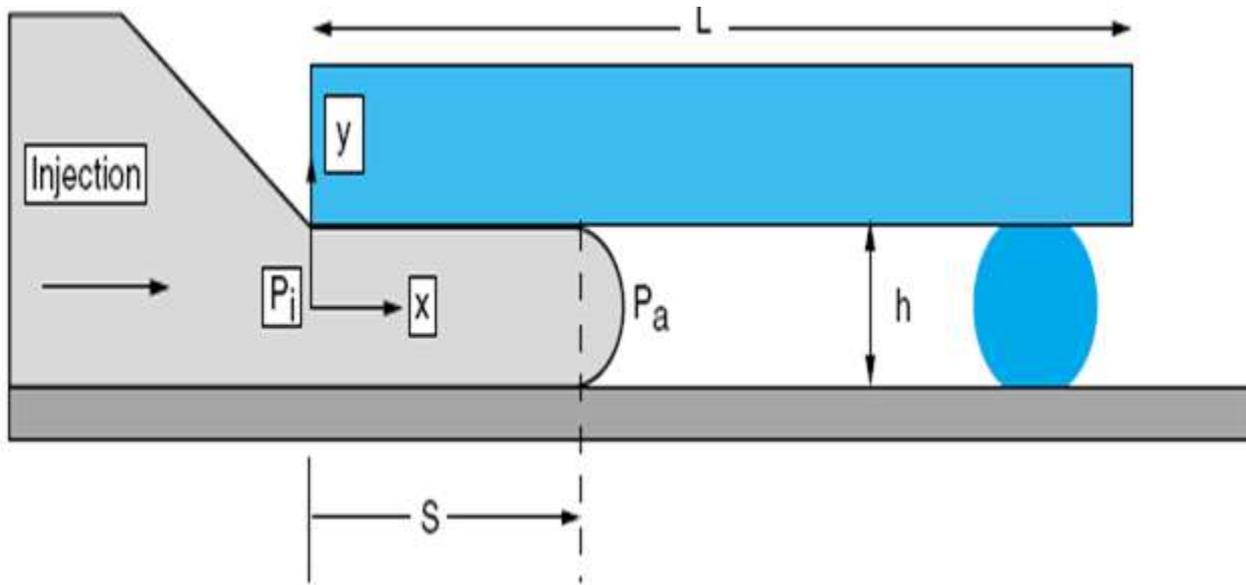
- Benefits
 - Cheaper
- Fall backs
 - High CTE
 - Fatigue
 - Bad joints
- IBM and Hitachi discovered that using polymer underfills reduce strain on solder

Underfill Encapsulants and Processing

- Advantages to underfills
 - Compensate for thermal expansion differences between chip and substrate
 - Avoid solder corrosion
 - Protect from environmental effects such as moisture
 - Absorb α particle emissions from lead in solder

Underfill Encapsulants and Processing





Underfill Encapsulants and Processing

- Compression Flow Processing
Placement velocity feedback

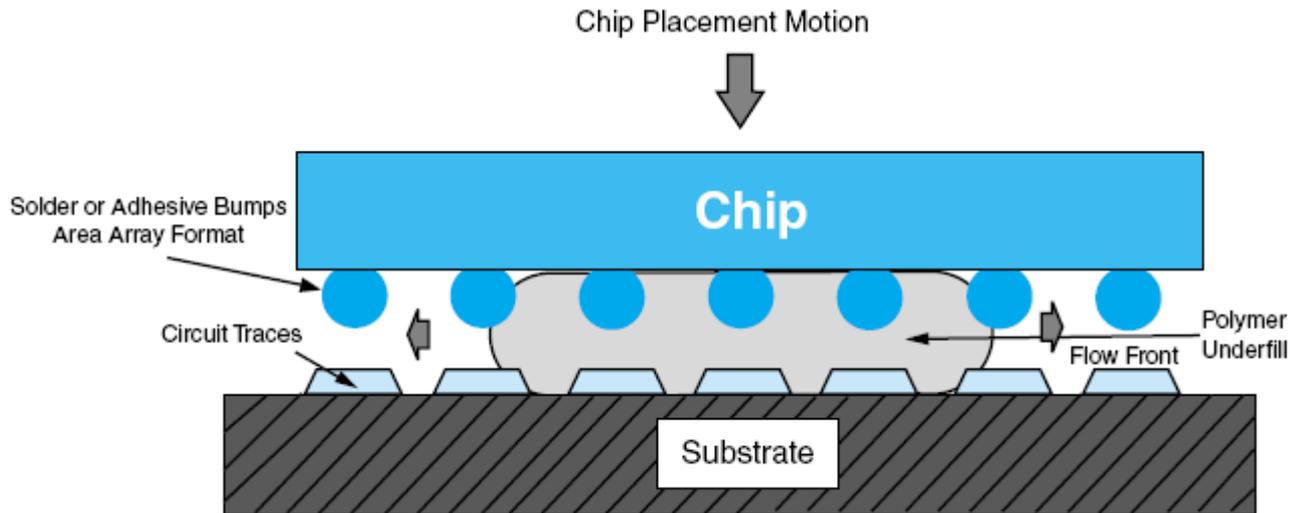
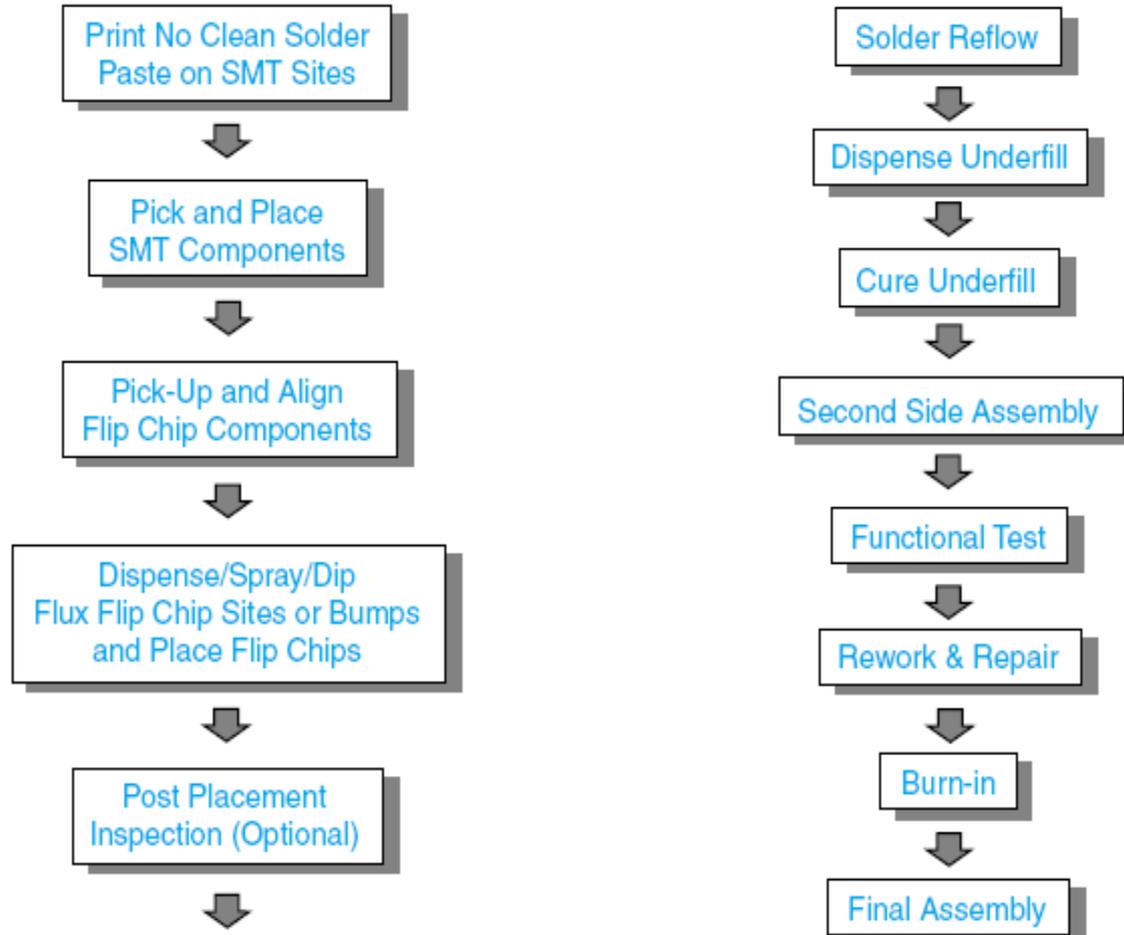


FIGURE 9.21 Compression flow underfill processing.

Flip Chip Assembly Processes



Electrical Performance

- Flip chip provide shortest chip-to-package connections
- Minimal resistance
- Minimal capacitance
- Minimal inductance
- Layout and materials effect the performance

Reliability

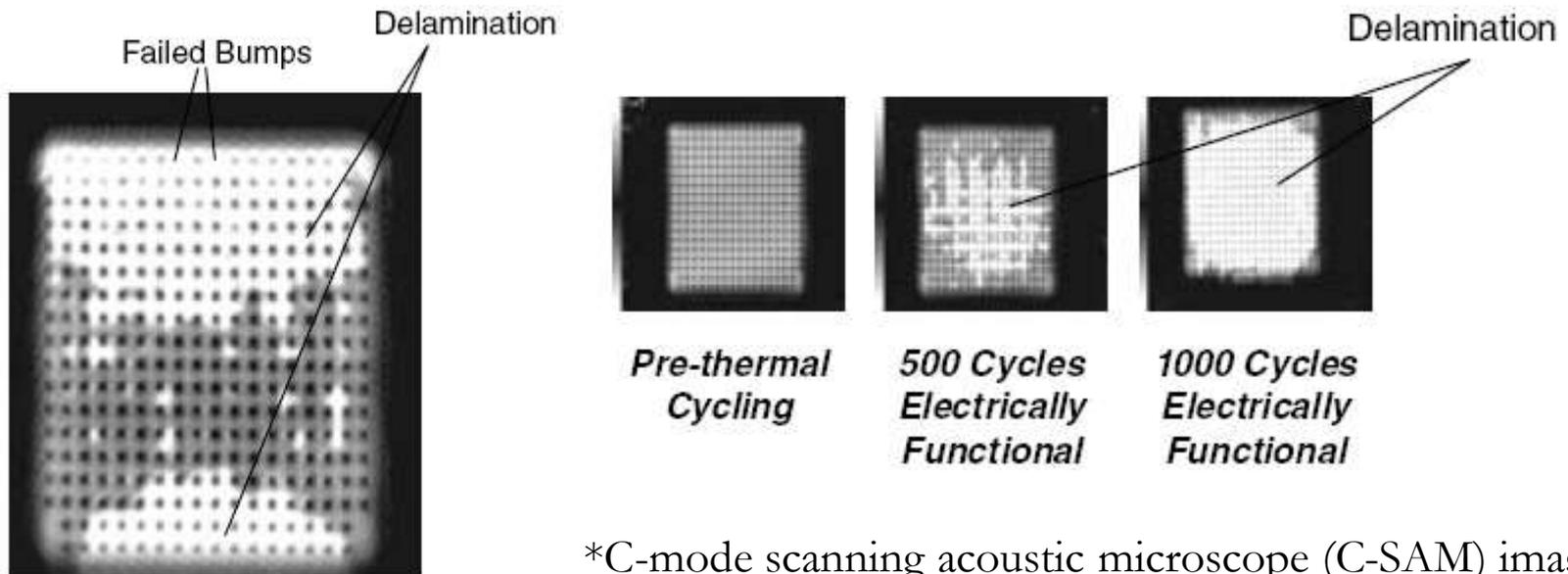
- Range from highly reliable to adequate
- Flip chips on ceramic have high reliability
- Underfilled flip chips have better reliability
- Alpha particle emissions (cause soft errors)
- Increased sensitivity to electrostatic discharge

Failure Modes

- **Delamination**

Increases solder joint stress

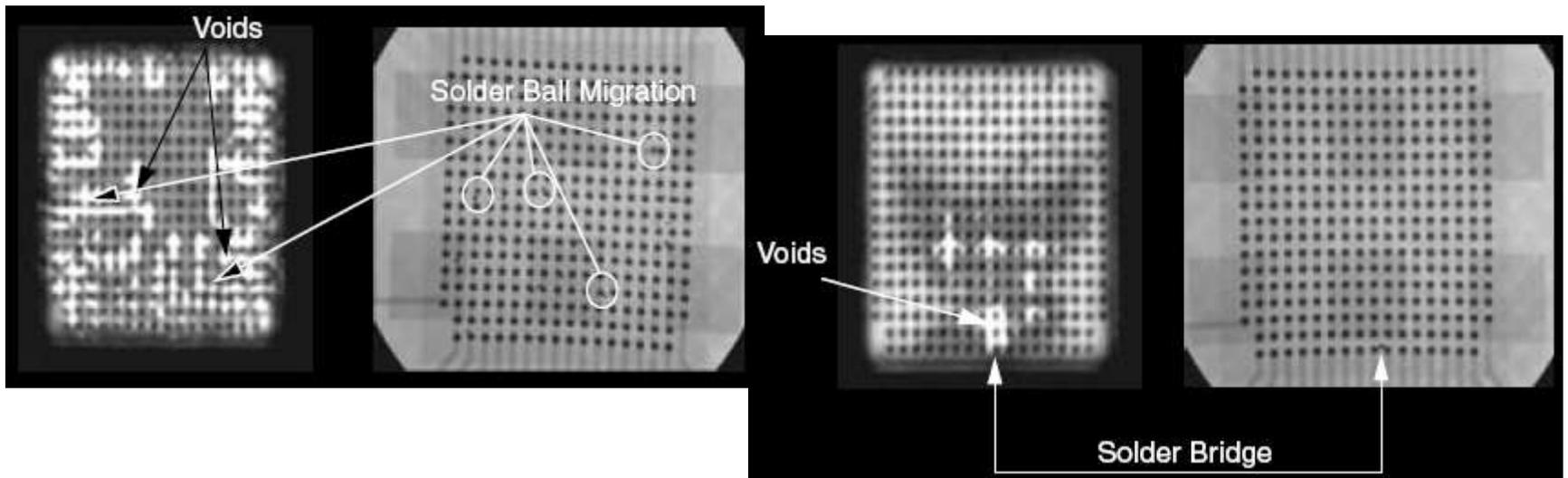
Allows solder to move into voids



*C-mode scanning acoustic microscope (C-SAM) images

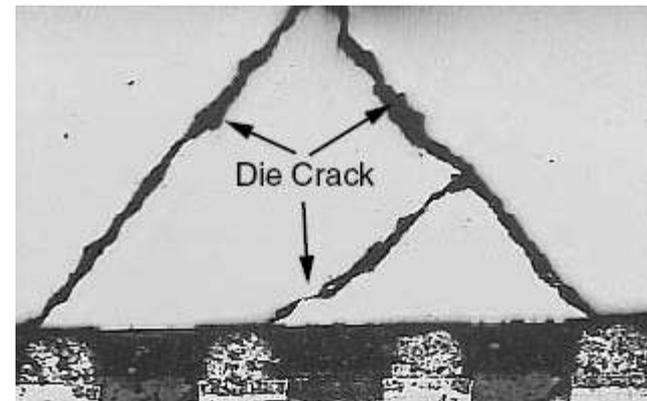
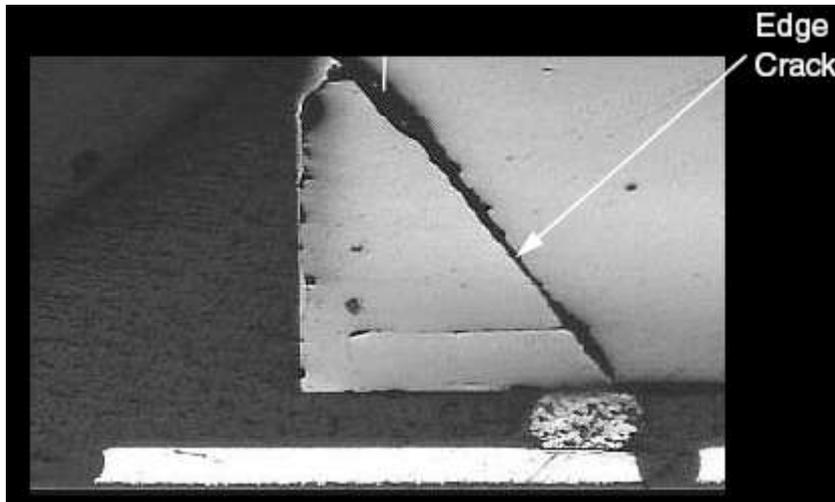
Failure Modes

- Solder migration
Can cause shorts by bridging



Failure Modes

- **Die cracking**
 - Catastrophic failure
 - Edge cracks
 - Center die cracks



Failure Modes

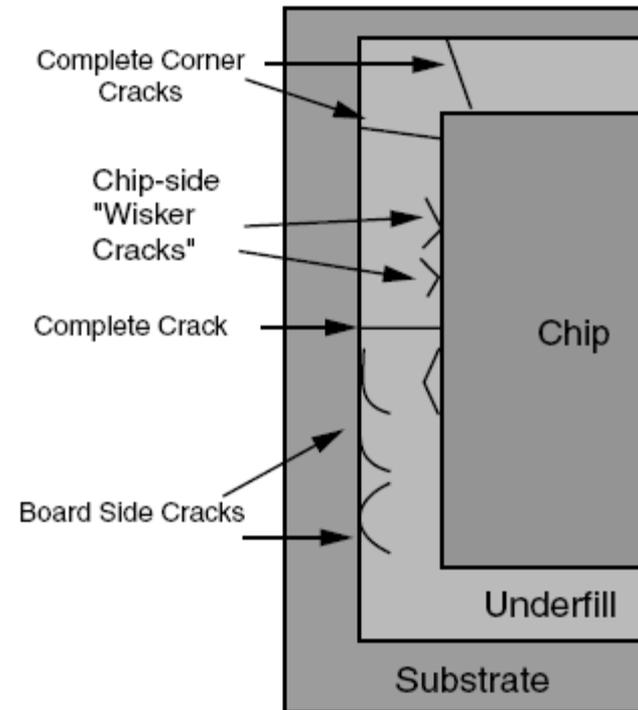
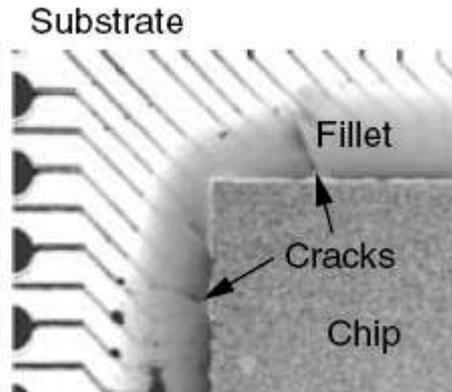
- **Fillet Cracking**

Chip side cracks

Board side cracks

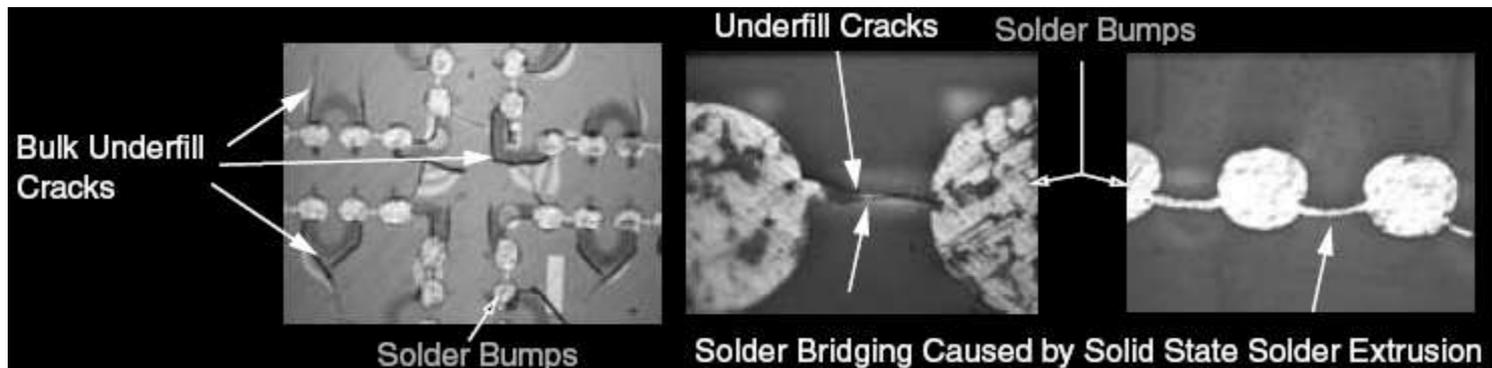
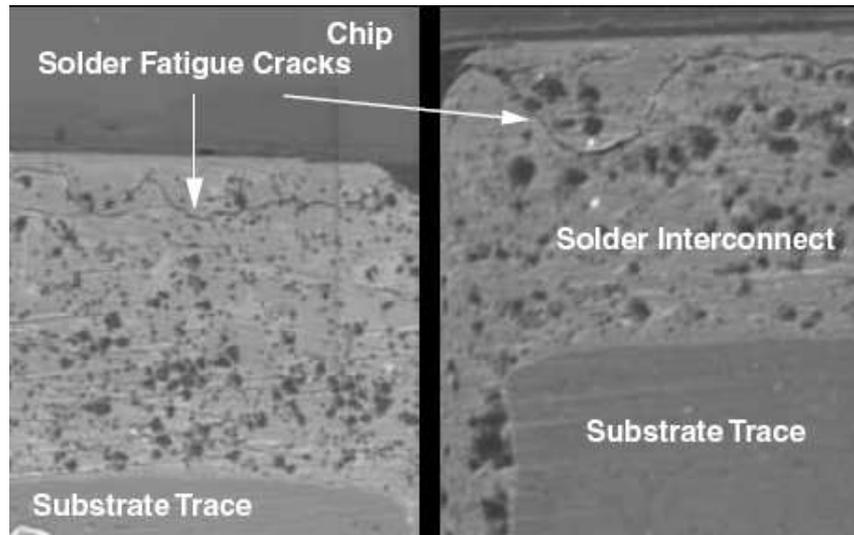
Complete cracks

Can lead to delamination



Failure Modes

- Solder fatigue cracking
 - Can create opens
- Bulk underfill cracking
 - Typically between joints
 - Potential to cause shorts



Speed up Flip Chip Process

- Use fast flow snap-cure underfills
- No flow underfills (adhesives)
- Remove steps from standard process

Do not use flux

Do not place explicit underfill fillets